**IN THE SPECIFICATION:**

Please amend the specification paragraph **[0015]** bridging pages 4 and 5 as follows:

-- In the detailed cross-sectional view of the DRAM structure 10 including storage cell MOSFET 20 and control cell ~~MOSFETs 20,~~ MOSFET 30 shown in Figure 1, each storage cell 20 and control cell ~~20,~~ 30 is formed on a substrate having an n-type doped region forming a buried plate 18. The storage cell device 25 further includes a source region 26 doped with n+ type material, a P-type well 45 and a drain diffusion region 28 doped of n+ type material. The capacitor 29 is a deep trench type formed within a substrate, having an isolated region 23 filled with polysilicon material. The polysilicon conductor is isolated with a collar dielectric material 46, e.g., an oxide, separating the drain diffusion from a buried plate region of n type silicon, for example. The gate 27 of the storage transistor 25 is isolated from the conductor 23 of the deep trench capacitor 29 by a top trench dielectric layer 24, e.g., an oxide. The control cell device 35 includes the buried strap 60 of n+-type material and with a gate 37 and a gate dielectric 34. The control cell gate 37 is connected to the n+ diffusion buried strap (BS2) 60 and influences a n-type doped diffusion layer 38 formed in a later thermal process in the p-well when receiving the WL voltage. That is, as will be described, in response to application of the wordline voltage, a depletion region is formed in the p-well 45 which functions to control p-well voltage and hence improve performance of the storage cell 20. --

Please amend paragraph **[0016]** on page 5 as follows:

--Figures 2(a) and 2(b) illustrate more clearly the operation of the novel DRAM control cell 30 for controlling the p-well voltage with Figure 2(a) illustrating a depletion region 75 formed in the p-well 45 at the location of the control cell 20 buried strap 60 for controlling p-well voltage when the WL is at an off state (e.g., WL at 0 volts). Figure 2(b) illustrates the depletion region 76 formed at the location of the control cell ~~20~~ 30 buried strap 60 for controlling p-well voltage when the WL is in an active state (e.g., WL at positive voltage such as 3 V – 4 V, for example). Particularly, as described with respect to Figures 2(a) and 2(b), when the p-well is connected [[at]] to a negative voltage supply having a value such as –0.5V, for example, and WL is at

ground, the lower buried strap 60 and resulting p-well depletion region 75 does not pinch off the p-type well 45. That is, at off-state, the control cell gate is at 0V, the depletion region 75 formed by the BS diffusion in the p-well does not block the path between p-well1 45a and p-well2 45b. Because of the body bias effect, a high enough Vt1 is achieved to achieve low off-state leakage current. As a result, the applied negative p-well voltage is sufficient to keep the Vt high enough to suppress the sub-threshold voltage in the storage cell MOSFET. --

Please amend paragraph **[0017]** bridging pages 5 and 6 of the specification as follows:

--As shown in Figure 2(b), when the WL is at an active state, the control cell ~~20~~ 30 buried strap 60 is at high voltage, the depletion region 76 formed between the BS 60 and p-well is sufficient to pinch off the top p-well (pass transistor p-well2) and bottom p-well (p-well1 connected to a contact). The p-well 45b will thus be at a floating state, thereby improving gate drive current. That is, when the gate is activated, the depletion regions between formed in the p-well at BS 60 extends sufficiently toward the storage cell collar dielectric 45 to render the top p-well1 45b at floating condition. Utilizing current doping profiles, the depletion width has at least a 50nm difference with WL at 3.0 volts versus 0.0 volts. Therefore, at this condition, the threshold voltage Vt2 is smaller than Vt1 and may range from 200 mV to 500 mV. Thus, the storage cell transistor can have more gate over drive and drive current.--